AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) A signal level detector comprising:

a first DC error amplifier operational to generate a output [control] signal in response to a reference signal and a feedback signal; and

a first inverter operational to generate the feedback signal in response to the first DC error amplifier output [control] signal, wherein the first DC error amplifier control signal operates to set a switching point for the first inverter;

a second DC error amplifier; [and]

a second inverter, wherein the first and second DC error amplifiers and the first and second inverters together implement a differential comparator generating a desired output signal in response to a differential input signal determined via the switching point associated with the first inverter and a switching point associated with the second inverter[.] and

a signal inverter coupled to the first DC error amplifier output signal to set a switching point for the signal inverter, the signal inverter operating as an open loop signal level detector; wherein an input signal is coupled ot the signal inverter for detecting a signal level of the input signal.

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Currently Amended) A signal level detector comprising:

first means for generating a first control signal in response to a first reference signal and further in response to a first feedback signal; and

second means for controlling the first feedback signal in response to the first control signal, wherein the first control signal operates to set a switching point for the second means;

third means for generating a second control signal in response to a second voltage reference signal and a second feedback signal; and

fourth means for controlling the second feedback signal in response to the second control signal, wherein the second control signal operates to set a switching point for the fourth means[,];

fifth means coupled to the first feedback signal to set a switching point for the fifth means;

sixth means coupled to the second feedback signal to set a switching point for the sixth means, [and further] wherein the first, second, third [and], fourth, fifth and sixth means together implement a differential comparator generating a desired output signal in response to a differential input signal voltage determined via the switching point associated with the second and fifth means and the switching point associated with the fourth and sixth means.

7. (Original) The signal level detector according to claim 6, wherein the third means for generating a second control signal comprises a DC error amplifier.

8. (Previously Presented) The signal level detector according to claim 6, wherein the fourth means for controlling the second feedback signal comprises a self-bias inverter.

9. (Cancelled)

10. (Currently Amended) A method of controlling a level detector, the method comprising the steps of:

providing a DC error amplifier having a positive input, a negative input and operational to generate [an] a first output control signal;

driving the negative input via a desired reference voltage; and

driving the positive input via a self-biasing inverter feedback signal in response to the first DC error amplifier output control signal to control a switching point associated with the self-biasing inverter;

providing a second DC error amplifier having a positive input, a negative input and operational to generate an output control signal;

driving the negative input of the second DC error amplifier via a second desired reference voltage; and

driving the positive input of the second DC error amplifier via a second self-biasing inverter feedback signal in response to the second DC error amplifier output control signal to control a switching point associated with the second inverter[.];

biasing a first signal inverter with the first DC error amplifier output control signal;

biasing a second signal inverter with the second DC error amplifier output control signal;

detecting a level of an input signal applied to inputs of the first and second signal inverters using the first and second signal inverters as open loop signal level detectors.

11. (Original) The method according to claim 10, further comprising the steps of:

providing output logic operational to generate a desired output signal in response to a differential input signal generated via the first and second DC error amplifiers; and

causing the desired output signal to change its logic state when the differential input signal reaches a desired difference level.